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NIT-83-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application:	Y. SASAKI et al Serial No. 08/930,219 Filed: October 20, 1997
Group Art Unit:	2763
Examiner:	H. Jones
For:	METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT AND AUTOMATIC DESIGNING DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure, the applicants inform the Examiner of the documents cited during prosecution of the parent application, Serial No. 08/930,219.

The above-referenced patent application is a continuation application of U.S. Application Serial No. 08/930,219, filed on October 20, 1997, from which priority is claimed under 35 U.S.C. § 120.

The applicants request the Examiner to initial and return a copy of the attached PTO-1449 form to indicate that the references have been considered.

Respectfully submitted,

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Registration No. 30,293
Attorney for Applicants

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Date: September 11, 2000

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. NIT-83-02	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT Y. SASAKI et al	
		FILING DATE 9/11/00	GROUP 2763

U. S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE *(If Appropriate)*
	AA	5,581,202	12/03/96	Yano et al			
	AB	4,477,904	10/16/84	Thorsrud			
	AC	5,144,582	09/01/92	Steele			
	AD	4,541,067	09/10/85	Whitaker			
	AE	5,243,538	09/07/93	Okuzawa et al			
	AF	5,649,165	7/97	Jain et al			
	AG	5,493,504	2/96	Minato			
	AH	4,912,348	3/90	Maki et al			
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		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL	4-160569	06/03/92	Japanese Laid-Open Patent				
	AM	6-215065	08/05/94	Japanese Laid-Open Patent				
	AN	6-20000	01/28/94	Japanese Laid-Open Patent				
	AO	7-168874	07/04/95	Japanese Laid-Open Patent				
	AP	4-112270	04/14/92	Japanese Laid-Open Patent				

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	AR		INFORMATION PROCESSING SOCIETY OF JAPAN, JOURNAL OF INFORMATION PROCESSING, Vol. 34, No. 5, May 1993, pp. 593-599.
	AS		INFORMATION PROCESSING SOCIETY OF JAPAN, PROCEEDINGS OF 1994 AUTUMN NATIONAL CONFERENCE, Vol. A, p. 64.
	AT		PROCEEDINGS OF IEEE 1994 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1994, PP. 603-606.

EXAMINER	DATE CONSIDERED

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	AM	1-256219	10/12/89	Japanese Laid-Open Patent				
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	AR		IEEE TRANSACTIONS ON COMPUTERS, Vol. C-35, No. 8, August, 1986, pp. 677-691.
	AS		PROCEEDINGS OF THE INFORMATION PROCESSING SOCIETY 44TH NATIONAL CONGRESS, PP. 6-143 TO 6-144.
	AT		IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-22, No. 2, April 1987, "CMOS Differential Pass-Transistor Logic Design", Pasternak et al, pp. 216-222.

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	AR		IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-25, No. 2, April 1990, "A 3.8-ns CMOS 16 x 16-b Multiplier Using Complementary Pass-Transistor Logic", Yano et al, pp. 388-395.
	AS		IEEE 1994 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1994 Digest, "Lean Integration: Achieving a Quantum Leap in Performance and Cost of Logic LSIs", Yano et al, pp. 603-606.
	AT		PROCEEDING OF THE 1994 AUTUMN CONVENTION OF THE INSTITUTE OF ELECTRONICS, INFORMATION AND COMMUNICATION ENGINEERS OF JAPAN, Edition of Fundamentals and Interfaces, page 64.

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	AR		IEEE TRANSACTIONS ON COMPUTERS, Vol. C-35, No. 8, August 1986, "Graph-Based Algorithms for Boolean Function Manipulation", R. Bryant, pp. 677-691.
	AS		DIGEST OF TECHNICAL PAPERS OF IEEE 1995 SYMPOSIUM ON LOW POWER ELECTRONICS, 1995, "Multi-Level Pass-Transistor Logic for Low-Power ULSIs", Y. Sasaki et al, pp. 14-15.
	AT		

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	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	AR		Tai: Pipelined Fault Simulation on Parallel Machines using the circuit flow graph; 1993 IEEE Int. Conf. on Comp. Design; pp. 564-567 10/93
	AS		Caban et al.; A parallel BDD engine for logic verification; 5th annual IEEE Int. ASIC Conf., pp. 499-502 9/92
	AT		Fujita et al.; Automatic and semi-automatic verification of switch-level circuits with temporal logic and binary decision diagrams; ICCAD-90; pp. 38-41 11/90

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